SPECIFICATIONS

PXIe-7912

KU040 FPGA, 4 GB DRAM, x8 Gen 3 PXI Coprocessor Module

This document lists the specifications for the PXIe-7912. Specifications are subject to change without notice. For the most recent device specifications, refer to *ni.com/support*.

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Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are *Typical* unless otherwise noted.

NATIONAL INSTRUMENTS

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature of 23 °C ± 5 °C
- Installed in chassis with slot cooling capacity ≥58 W

Digital I/O

Connector	Molex™ Nano-Pitch I/O™
5 V Power	5.0 V DC, ±5%, nominal 50 mA maximum

Table 1. Digital I/O Signal Characteristics

Signal	Type	Direction
Multi-gigabit transceivers (MGT) Tx± <3..0>	Xilinx UltraScale GTH	Output
MGT Rx± <3..0>	Xilinx UltraScale GTH	Input
DIO <7..0>	Single-ended	Bidirectional
5 V	DC	Output
GND	Ground	—

Digital I/O Single-Ended Channels

Number of channels	8
Signal type	Single-ended
Voltage families	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V
Input impedance	100 kΩ, nominal
Output impedance	50 Ω, nominal
Direction control	Per channel
Minimum required direction change latency	200 ns
Maximum output toggle rate	60 MHz with 100 μA load, nominal

Table 2. Digital I/O Single-Ended DC Signal Characteristics[1]

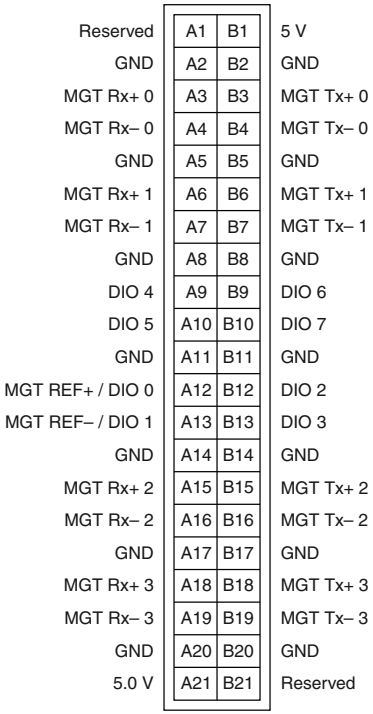
Voltage Family	V_{IL}	V_{IH}	V_{OL} (100µA load)	V_{OH} (100µA load)	Maximum DC Drive Strength
3.3 V	0.8 V	2.0 V	0.2 V	3.0 V	24 mA
2.5 V	0.7 V	1.6 V	0.2 V	2.2 V	18 mA
1.8 V	0.62 V	1.29 V	0.2 V	1.5 V	16 mA
1.5 V	0.51 V	1.07 V	0.2 V	1.2 V	12 mA
1.2 V	0.42 V	0.87 V	0.2 V	0.9 V	6 mA

Digital I/O High-Speed Serial MGT[2]

Data rate	500 Mbps to 16.375 Gbps, nominal
Number of Tx channels	4
Number of Rx channels	4

[1] Voltage levels are guaranteed by design through the digital buffer specifications.
[2] For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.

Figure 1. Digital I/O Connector



MGT TX± Channels

Minimum differential output voltage[3]	170 mV pk-pk into 100 Ω, nominal
I/O coupling	AC-coupled with 100 nF capacitor

MGT RX± Channels

Differential input voltage range	
≤ 6.6 Gb/s	150 mV pk-pk to 2000 mV pk-pk, nominal
> 6.6 Gb/s	150 mV pk-pk to 1250 mV pk-pk, nominal
Differential input resistance	100 Ω, nominal
I/O coupling	DC-coupled, requires external capacitor ⚠

[3] 800 mV pk-pk when transmitter output swing is set to the maximum setting.

Reconfigurable FPGA

FPGA	Xilinx KU040
LUTs	242,200
DSP48 Slices (25 × 18 multiplier)	1,920
Total block RAM	21.1 Mb
Default timebase	80 MHz
Timebase reference sources	PXI Express 100 MHz (PXIe_CLK100)
Data transfers	MGT
Number of DMA channels	60
Connection resources	PXI triggers, PXI_CLK10, PXI star trigger, PXIe_DStarB, PXIe_DStarC, and PXIe_Sync100

Note The preceding specifications describe the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI support.

Note For FPGA designs using the majority of KU040 or KU060 FPGA resources while running at clock rates over 150 MHz, the module may require more power than is available. If the module attempts to draw more than allowed per its specification, the module protects itself and reverts to a default FPGA personality. Refer to the getting started guide for your module or contact NI support for more information.

Onboard DRAM

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit
LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)

Driver and Application Software

This device is supported in NI LabVIEW Instrument Design Libraries for FlexRIO (instrument design libraries). Instrument design libraries allow you to configure and control the device.

The instrument design libraries provide programming interfaces, documentation, and sample projects for LabVIEW and LabVIEW FPGA Module.

Bus Interface

Form factor	PCI Express Gen-3 x8

Maximum Power Requirements

Note Power requirements are dependent on the contents of the LabVIEW FPGA VI used in your application.

+3.3 V	3 A
+12 V	4 A
Maximum total power	58 W

Physical

Dimensions (not including connectors)	18.8 cm × 12.9 cm (7.4 in. × 5.1 in.)
Weight	190 g (6.7 oz)

Note Clean the hardware with a soft, nonmetallic brush. Make sure that the hardware is completely dry and free of contaminants before returning it to service.

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C[4]
Relative humidity range	10% to 90%, noncondensing

Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 4 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 g_{rms} (Tested in accordance with IEC 60068-2-64.)
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

[4] The PXIe-7912 requires a chassis with slot cooling capacity ≥58 W. Not all chassis with slot cooling capacity ≥58 W can achieve this ambient temperature range. Refer to the *PXI Chassis Manual* for specifications to determine the ambient temperature ranges your chassis can achieve.

376456B-01 January 28, 2020